AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (original): A current detection circuit, characterized by comprising:

a first transistor for supplying load current to a load;

a current detection transistor having a control electrode receiving the same control signal as applied to the control electrode of said first transistor, said current detection transistor adapted to supply a proportional current that is proportional to said load current;

a buffer circuit having an idling current source for supplying a predetermined idling current to an output node of said current detection transistor, said buffer circuit adapted to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current; and

a conversion circuit for converting into an output signal said detection current outputted from said buffer circuit.

Claim 2 (original): A current detection circuit, characterized by comprising:

a current controlling transistor having a control electrode and an output electrode connected to said control electrode;

a variable-current type control-current supplying current source for flowing controlled current through said current controlling transistor;

a first transistor connected to said current controlling transistor in a current mirror configuration for supplying load current to a load;

a current detection transistor connected to said current controlling transistor in a current mirror configuration for supplying a proportional current that is proportional to said load current;

a buffer circuit having an idling current source for providing a predetermined idling current to the output node of said current detection transistor, said buffer circuit adapted to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current; and

a conversion circuit for converting into an output signal said detection current outputted from said buffer circuit.

Claim 3 (currently amended): The current detection circuit according to claim 1 ~~or claim 2~~, characterized in that said buffer circuit has:

an amplifier fed with the output voltage of said first transistor and the voltage appearing at the output node of said current detection transistor; and

a third transistor provided between said output node of said current detection transistor and said conversion circuit, and controlled by the output of said amplifier.

Claim 4 (currently amended): The current detection circuit according to claim 1 ~~or claim 2~~, characterized in that the power supply voltage supplied to said idling current source is equal to or higher than the first power supply voltage supplied to said first transistor and said current detection transistor.

Claim 5 (currently amended): The current detection circuit according to claim 1 ~~or claim 2~~, characterized by further comprising:

a switching circuit provided in said idling current source;

a comparator for generating a comparison output to switch off said switching circuit when said output signal exceeds a reference level.

Claim 6 (original): The current detection circuit according to claim 5, characterized in that said comparator has a characteristic hysteresis having a predetermined hysteresis width.

Claim 7 (currently amended): The current detection circuit according to claim 1 ~~or 2~~, characterized by further comprising:

a switching circuit provided in said idling current source and switched on by an idling signal; and

a timing circuit for outputting said idling signal for a first predetermined period of time upon receipt of said control command signal and for outputting said control signal after a second predetermine time has elapsed since the receipt of said control command signal, said second predetermine time being shorter than said first predetermined time.

Claim 8 (original): A load drive circuit for performing pulse-width-modulated (PWM) driving of a single-/multi-phase load, said load drive circuit having at least two series circuits such that each of said series circuits includes: a first transistor coupled between a first power supply voltage and the output node connected to said load to supply load current to said load when switched on by a switching signal; and a second transistor coupled between a second power supply voltage and said output node and switched on and off by a PWM switching signal, and that said series circuits together form a single-/multi-phase bridge circuit for driving said single-/multi-phase load, said load drive circuit characterized in that:

each of said series circuits comprises:

a current detection transistor receiving the same switching signal as the switching signal supplied to said first transistor to provide a proportional current proportional to said load current; and

a buffer circuit having an idling current source for providing a predetermined idling current to the output node of said current detection transistor, said buffer circuit adapted to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current, and characterized in that

said load drive circuit further comprises a conversion circuit for collectively

converting into an output signal the detection currents outputted from the respective buffer circuits.

Claim 9 (original): A load drive circuit having at least two current output circuits to form a single-/multi-phase bridge circuit for driving a single-/multi-phase load, each of said current output circuits including: a current controlling transistor having a control electrode and an output electrode connected to said control electrode;=control-current supplying current source for supplying controlled current to said current controlling transistor; a first transistor connected to said current controlling transistor in a current mirror configuration and provided between a first power supply voltage and the output node of said load drive circuit supplying load current to said load; and a second transistor connected between said output node and a second power supply voltage and configured to be switched on and off by a switching signal, said load drive circuit characterized in that

each of said current outputting circuit comprises, in association with the first transistor thereof:

a current detection transistor, connected to said current controlling transistor in a current mirror configuration for supplying a proportional current that is proportional to said load current; and

a buffer circuit having an idling current source for providing a predetermined idling current to the output node of said current detection transistor, said buffer circuit adapted to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current, and characterized in that

said load drive circuit comprises a conversion circuit for collectively converting the detection currents outputted from the respective buffer circuits into an output signal.

Claim 10 (currently amended): The load drive circuit according to claim 8 ~~or claim 9~~, characterized in that said buffer circuit has:

an amplifier fed with the output voltage of said first transistor and the voltage appearing at the output node of said current detection transistor; and

a third transistor provided between said output node of said current detection transistor and said conversion circuit, and controlled by the output of said amplifier.

Claim 11 (currently amended): The load drive circuit according to claim 8 ~~or claim 9~~, characterized by further comprising:

a switching circuit provided in said idling current source; and

a comparator for generating a comparison output when said output signal exceeds said reference level, to thereby switch off said switching circuit by said comparison output.

Claim 12 (currently amended): The load drive circuit according to claim 8 ~~or claim 9~~, characterized by further comprising:

a switching circuit provided in said idling current source and switched on by an idling signal; and

a timing circuit for outputting said idling signal for a first predetermined period of time upon receipt of said control command signal and for outputting said control signal after a second predetermine time has elapsed since the receipt of said control command signal, said second predetermine time being shorter than said first predetermined time.

Claim 13 (currently amended): A memory storage characterized by comprising:

a load drive circuit in accordance with ~~any one of~~ claim~~s~~ 8~~-12~~; and

a motor driven by said load drive circuit.